Bottom-gated P(VDF-TrFE) ferroelectric memory transistor with a 2D channel

Yongjae Cho*, Seongil Im*

* Department of Physics, Yonsei University, Seoul
Email: semicon@yonsei.ac.kr

$MoTe_2$ channel-based P(VDF-TrFE) ferroelectric nonvolatile memory is fabricated, which operates at minimum switching pulse voltage and minimum drain voltage. For the minimum switching voltage of 8 V, bottom-gate architecture is employed, and its advantages are investigated. By using bottom-gate structure, we could avoid a dead layer formed at the interface between thermally-deposited Al and P(VDF-TrFE) at top-gate architecture. A dead layer in top-gated ferroelectric memory transistors increases the coercive voltage so as the switching pulse voltage. And, for the minimum drain voltage, a novel method of H_2O_2 treatment is developed. By oxidizing the source/drain area of $MoTe_2$ surface by H_2O_2 solution, Ohmic contact between Pt and $MoTe_2$ is achieved even without thermal annealing which would have a destructive effect on the crystal quality of P(VDF-TrFE). To demonstrate the benefit of our memory transistor in aspect of power saving, it is integrated into an OLED operating circuit.

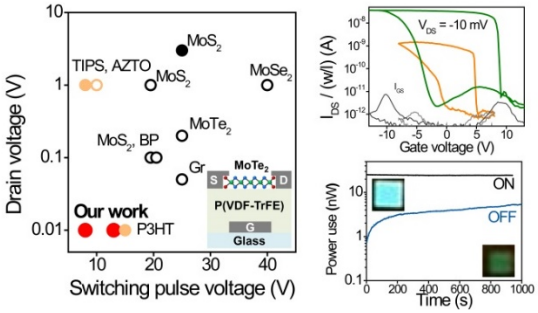

Fig. 1. Comparison plot showing switching pulse and drain/operation voltages of reported nonvolatile memory FETs, Memory hysteresis transfer and displacement characteristics, Power consumption-time plots of memory FETs